## ABSTRACT OF THE DISCLOSURE

A device for use in a digital video receiver. The device generally comprising a demodulator circuit, a decoder circuit, a plurality of bi-directional buffers, and a circuit. The demodulator circuit may be configured to generate (i) a first clock signal compliant with a standard interface for the digital video receiver and (ii) a first plurality of data signals compliant with the standard interface. The decoder circuit may be configured to receive a second plurality of data signals compliant with the standard interface. The plurality of first bi-directional buffers may be configured to multiplex the first data signals with the second data signals at a plurality of data interfaces in response to the first clock signal. The circuit may be configured to generate a direction signal at a direction interface in response to the first clock signal to indicate a direction of the data interfaces.